CLAIMS

Sub A1

1. A semiconductor processing method, comprising:

forming an insulative mass across a first electrical node and a second electrical node; the mass having a pair of openings extending therethrough to the electrical nodes; the individual openings each having a periphery defined by at least a portion of one of the electrical nodes and at least one sidewall; one of the openings extending to the first electrical node and being a first opening, and the other of the openings extending to the second electrical node and being a second opening;

forming a dielectric material layer within the openings to narrow the openings; and

forming conductive material plugs within the narrowed openings; the conductive material plug within the first opening being a first conductive material plug and being separated from the first electrical node by the dielectric material, and the conductive material plug within the second opening being a second conductive material plug and not being separated from the second electrical node by the dielectric material.

2. The method of claim 1 wherein the insulative mass comprises borophosphosilicate glass.

3. The method of claim 1 wherein the dielectric material layer comprises silicon nitride.

4. The method of claim 1 wherein the dielectric material layer comprises silicon oxynitride.

5. The method of claim 1 wherein the dielectric material layer comprises silicon nitride and is formed to a thickness of from about 30Å to about 100Å.

6. The method of claim 1 wherein the first electrical node comprises a p-type doped diffusion region within a semiconductive material.

7. The method of claim 1 wherein the first electrical node comprises an n-type doped diffusion region within a semiconductive material.

8. The method of claim 1 wherein the first electrical node comprises a metal.

9. The method of claim 1 wherein the first electrical node comprises copper.

10. The method of claim 1 wherein the first electrical node comprises aluminum.

11. The method of claim 1 wherein the first electrical node comprises copper and aluminum.

12. The method of claim 1 wherein the conductive plugs comprise conductively doped silicon.

13. The method of claim 1 wherein the conductive plugs comprise a metal.

14. The method of claim 1 wherein the conductive plugs comprise tungsten.

15. The method of claim 1 wherein the conductive plugs comprise copper.

16. The method of claim 1 wherein the conductive plugs comprise aluminum.

17. The method of claim 1 wherein the conductive plugs comprise copper and aluminum.

18. The method of claim 1 wherein the conductive plugs comprise a layer of titanium nitride against the dielectric material; and a mass of tungsten over the layer of titanium nitride.

19. The method of claim 1 wherein the conductive plugs comprise a composite layer of titanium and titanium nitride against the dielectric material; and a mass of tungsten over the composite layer of titanium and titanium nitride.

20. A semiconductor processing method, comprising:

forming an insulative mass across a first electrical node and a second electrical node; the mass having a pair of openings extending therethrough to the electrical nodes; the individual openings each having a periphery defined by at least a portion of one of the electrical nodes and at least one sidewall; one of the openings extending to the first electrical node and being a first opening, and the other of the openings extending to the second electrical node and being a second opening;

forming a dielectric material layer within the openings to narrow the openings; and

forming conductive material plugs within the narrowed openings; the conductive material plug within the first opening being a first conductive material plug and not being in electrical contact with the first electrical node, and the conductive material plug within the second opening being a second conductive material plug and being in electrical contact with the second electrical node.

21. The method of claim 20 wherein the insulative mass comprises borophosphosilicate glass.

22. The method of claim 20 wherein the dielectric material layer comprises silicon nitride.

23. The method of claim 20 wherein the dielectric material layer comprises silicon nitride and is formed to a thickness of from about 30Å to about 100Å.

24. A semiconductor processing method, comprising:

providing a semiconductor substrate having a pair of electrical nodes supported thereby; the electrical nodes being a first electrical node and a second electrical node, respectively;

forming an insulative mass over the substrate; the mass having a pair of openings extending therethrough to the electrical nodes; the individual openings each having a periphery defined by a bottom and at least one sidewall; the opening extending to the first electrical node being a first opening, and the opening extending to the second electrical node being a second opening;

forming a dielectric material layer within the openings to narrow the openings; the dielectric material layer lining the at least one sidewall and bottom of the first opening, and lining the at least one sidewall but not a predominant portion of the bottom of the second opening; and

forming conductive material plugs within the narrowed openings; the conductive material plug within the first opening being a first conductive material plug, and the conductive material plug within the second opening being a second conductive material plug.

25. The method of claim 24 wherein an anti-fuse is defined by the first electrical node together with the dielectric material layer in the first opening and the first conductive material plug; and further comprising providing sufficient power to the anti-fuse to electrically connect the first electrical node and first conductive material plug to one another.

26. The method of claim 24 wherein the forming the dielectric material layer comprises:

forming the dielectric material layer along the at least one sidewall of the second opening and along the bottom of the second opening while forming the dielectric material layer along the at least one sidewall and along the bottom of the first opening;

forming a protective mask over the first opening and leaving the second opening uncovered by the protective mask; and

while the protective mask is over the first opening; anisotropically etching the dielectric material layer from over the predominant portion of the bottom of the second opening.

27. The method of claim 24 wherein the dielectric material layer comprises silicon nitride.

28. The method of claim 24 wherein the dielectric material layer comprises silicon nitride and is formed to a thickness of from about 30Å to about 100Å.

29. The method of claim 24 wherein the first electrical node comprises a p-type doped diffusion region within a semiconductive material of the semiconductor substrate.

30. The method of claim 24 wherein the first electrical node comprises an n-type doped diffusion region within a semiconductive material of the semiconductor substrate.

31. The method of claim 24 wherein the first electrical node comprises a metal.

32. The method of claim 24 wherein the first electrical node comprises copper.

33. The method of claim 24 wherein the first electrical node comprises aluminum.

34. The method of claim 24 wherein the first electrical node comprises copper and aluminum.

35. The method of claim 24 wherein the conductive plugs comprise conductively doped silicon.

36. The method of claim 24 wherein the conductive plugs comprise a metal.

37. The method of claim 24 wherein the conductive plugs comprise tungsten.

38. The method of claim 24 wherein the conductive plugs comprise copper.

39. The method of claim 24 wherein the conductive plugs comprise aluminum.

40. The method of claim 24 wherein the conductive plugs comprise copper and aluminum.

41. The method of claim 24 wherein the conductive plugs comprise a layer of titanium nitride against the dielectric material; and a mass of tungsten over the layer of titanium nitride.

42. A semiconductor assembly, comprising:

a semiconductor substrate having a pair of electrical nodes supported thereby; the electrical nodes being a first electrical node and a second electrical node, respectively;

an insulative mass over the substrate; the mass having a pair of openings extending therethrough to the electrical nodes; the individual openings each having a periphery defined by a bottom and at least one sidewall; the opening extending to the first electrical node being a first opening, and the opening extending to the second electrical node being a second opening;

a dielectric material layer within the openings; the dielectric material layer lining the at least one sidewall and bottom of the first opening, and lining the at least one sidewall but not a predominant portion of the bottom of the second opening;

conductive material plugs within the openings; the conductive material plug within the first opening being a first material plug, and the conductive material plug within the second opening being a second material plug; the first and second conductive material plugs comprising the same chemically constituencies as one another;

the first electrical node, dielectric material within the first opening, and first conductive material plug together being incorporated into an anti-fuse construction; and

the second electrical node, dielectric material within the second opening, and second conductive material plug together being incorporated into an electrically conductive interconnect construction.

43. The assembly of claim 42 wherein the dielectric material layer comprises silicon nitride.

44. The assembly of claim 42 wherein the both conductive plugs are formed by common and simultaneous processing.

45. The assembly of claim 42 wherein the dielectric material is formed within the pair of openings by common and simultaneous processing.

46. The assembly of claim 42 wherein the dielectric material layer comprises silicon nitride and has a thickness of from about 30Å to about 100Å.

47. The assembly of claim 42 wherein the first electrical node comprises a p-type doped diffusion region within a semiconductive material of the semiconductor substrate.

48. The assembly of claim 42 wherein the first electrical node comprises an n-type doped diffusion region within a semiconductive material of the semiconductor substrate.

49. The assembly of claim 42 wherein the first electrical node comprises a metal.

50. The assembly of claim 42 wherein the first electrical node comprises copper.

51. The assembly of claim 42 wherein the first electrical node comprises aluminum.

52. The assembly of claim 42 wherein the first electrical node comprises copper and aluminum.

53. The assembly of claim 42 wherein the conductive plugs comprise conductively doped silicon.

54. The assembly of claim 42 wherein the conductive plugs comprise a metal.

55. The assembly of claim 42 wherein the conductive plugs comprise tungsten.

56. The assembly of claim 42 wherein the conductive plugs comprise copper.

57. The assembly of claim 42 wherein the conductive plugs comprise aluminum.

58. The assembly of claim 42 wherein the conductive plugs comprise copper and aluminum.

59. The assembly of claim 42 wherein the conductive plugs comprise a layer of titanium nitride against the dielectric material; and a mass of tungsten over the layer of titanium nitride.